Isolated Dual-Core Redundant Security Processor

Zero Sharing, Total Isolation

Separation by architecture, security by design.

ERGTECH Research GmbH

prigm

A physically partitioned RISC-V SoC where Red and Black security domains share no cache, no bus, and no silicon — separated by a cycle-accurate dual-redundant cryptographic boundary.

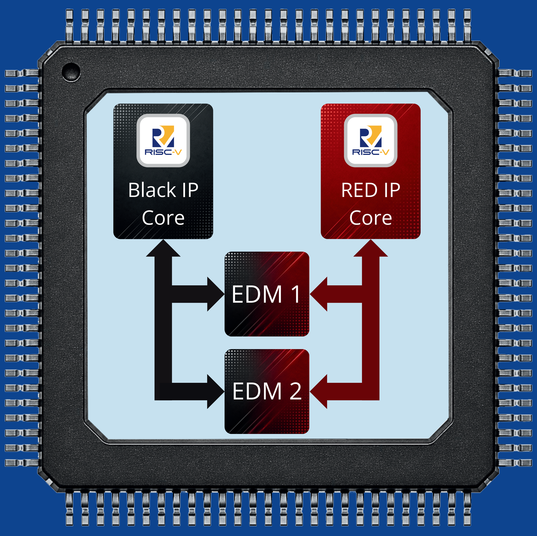
Asymmetric Isolated Cores

DMR Crypto Accelerator

Zero Shared Microarchitectural State

Linux-Ready RV64GC

Climbing Up Towards a Novel RISC-V Trusted Execution Environment with a Strong Vision to Use in Various Application Areas



Ready for Integration with AI Accelerators

Compliant with Post-Quantum Cryptography (PQC)

Key Capabilities

Zero shared microarchitectural state
No cache, branch predictor, or interconnect state is shared between Red and Black at any level

Hardware-verified dual EDM boundary
EDMs working in parallel and hardware-compared before any data crosses the domain boundary

On-Chip True Random Number Generator
Passing the full NIST-800-22 test suite at high throughput.

Post-quantum cryptography ready
EDM algorithm suite designed to accommodate PQC primitives as standardisation matures.

Transient execution resistant
Eliminates cross-domain speculation channels without software mitigations.

Dedicated peripherals per domain
Red and Black domains remain isolated at every level, including I/O.

Reference EU Projects

RIGOLETTO HIGH PERFORMANCE RISC-V SOLUTIONS

AI4SWEng

NexTArc

PQComing

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