LLM-Driven RTL Automation

AI-Assisted Hardware Design with Verification and Traceability

From engineer intent to validated, traceable RTL evidence.

A verification-gated AI architecture that combines LLMs, specialist agents, and industry-standard EDA tools to deliver reliable, traceable hardware design artifacts for RISC-V systems.

Engineer-Controlled | **Verification-Gated** | **Traceable by Design** | **RISC-V Native**

ENGINEER INTENT
Natural-Language Design Request

↓

ORCHESTRATION LAYER
Plan, Monitor, Review

↓

SPECIALIST AGENT LAYER
RTL, Verification, Synthesis and Constraints Agents

↓

EDA TOOL LAYER
Verilator, cocotb, Yosys

↓

EVIDENCE-GATED DECISION
Approve, Reject, Block, Repair

↓

TRACEBLE-OUTPUT PACKAGE
RTL, Tests, Reports, Ontology Trace

KNOWLEDGE SUBSTRATE

Ontology
Captures domain knowledge, requirements, design relationships and rules

RAG Store
Retrieves relevant knowledge and past solutions for better generation.

Local/Fine-tuned Models
Optimized for hardware design, private and secure.

Why?

ONLY ENGINEER
Manual coding/testing/tool runs/documentation/review
Time consuming. Error-prone and hard to scale.

ONLY LLM
Fast RTL candidate; Missing Tests; No real tool validation; No traceability; Weak model confidence
Unverified, non-deterministic and not production-ready.

LLM-Driven RTL Automation
Structured plan, RTL and test generation; Automated EDA validation; Deterministic decisions; Validation Evidence
Verified, traceable and engineer-controlled.

Key Capabilities

Natural-Language Engineering
Express complex hardware ideas in plain English.

Ontology-Aware Planning
Understands domain knowledge and existing design patterns.

RTL Candidate Generation
Generated synthesizable, well-structured RTL with explanations.

EDA Validation
Verilator linting, cocotb simulation and other tools generate objective evidence.

Deterministic Monitor Decision
Rule-based acceptance or rejection ensures reliability.

Traceability by Design
Automatic JSON-LD export links requirement to every decision and artifact.

Reference EU Projects

RIGOLETTO HIGH PERFORMANCE RISC-V SOLUTIONS | AI4SWENG | NexTArc | dPQComing

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